



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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4-15-03

Applicant(s): Longden et al.

Appl. No.: 10/065,209

Filed: 9/25/2002

Title: METHOD AND APPARATUS FOR
SHIELDING AN INTEGRATED
CIRCUIT FROM RADIATION

Group Art Unit: TBA

Examiner: TBA

Attorney Docket No.: 73591

Commissioner for Patents
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

This Information Disclosure Statement is submitted:

☒ under 37 CFR 1.97(b), or
(Within three months of filing national application; or date of entry of international application; or before mailing date of first office action on the merits; whichever occurs last)

☐ under 37 CFR 1.97(c) together with either a:
☐ Statement under 37 CFR 1.97(e), or
☐ a \$180.00 fee under 37 CFR 1.17(p), or
(After the CFR 1.97(b) time period, but before final action or notice of allowance, whichever occurs first)

☐ under 37 CFR 1.97(d) together with a:
☐ Statement under 37 CFR 1.97(e), and
☐ a \$180.00 fee set forth in 37 CFR 1.17(p).
(Filed after final action or notice of allowance, whichever occurs first, but before payment of the issue fee)

☒ Applicant(s) submit herewith Form PTO 1449-Information Disclosure Citation together with copies, of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.



listed on PTO-1449 are either in the English language or an English translation is provided hence, no further explanation is required, with exception to the following non-English references. A concise explanation, as presently understood, is as follows:

Japanese Patent Publication No. 60-180150 appears to disclose a semiconductor device enclosed within a plastic package, and surrounded by a thin metallic plating to absorb or collect unwanted electro-magnetic interference (EMI). The reference appears to concentrate on preventing malfunctions due to EMI, and does not appear to discuss spacecraft environment hazards, including high energy electron, proton and cosmic ray damage. The Applicant does not currently possess an English translation of this document.

Japanese Patent Publication No. 61-004249 appears to disclose a spot shielded semiconductor device which utilizes a single-layer shield film. The reference appears to concentrate on the use of a shield composed of Cu-W alloy and does not appear to discuss a shielded semiconductor device which provides approximately 4pi protection for the semiconductor device. Applicant does not currently possess an English translation of this document.

Japanese Patent Publication No. 62-125651 appears to disclose the use of spot shielding to protect a semiconductor device. The reference appears to concentrate on attaching a double-layered shield film to a sealing cover on an upper surface of the semiconductor package, and attaching another double-layered shield film to a lower surface of the package. The reference does not appear to discuss the use of a single-layer shield to reduce the weight of the semiconductor device, and to reduce the likelihood of the shield becoming dislodged from the semiconductor device during periods of high gravitational forces being applied to the device. Applicant does not currently possess an English translation of this document.

The relevance of the attached references is that this is the closest art of which Applicant is aware. Applicant submits that the above references taken alone or in combination neither anticipate nor render obvious the present invention. Consideration of the foregoing in relation to this application is respectfully requested.

It is requested that the information disclosed herein be made of record in this application.

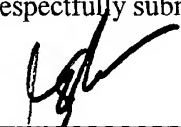
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231.

Date of Deposit: November 26, 2002

Typed Name: Thomas F. Lebens

Signature: 

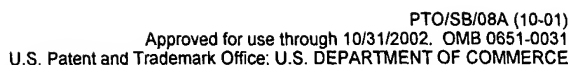
Respectfully submitted,


Thomas F. Lebens
Attorney/Agent for Applicant(s)
Reg. No. 38221

Date: November 26, 2002

Telephone No.: 805-781-2865

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Substitute for form 1449A/PTO				Complete if Known Application Number 10/065,209 Filing Date 9/25/2002 First Named Inventor Longden et al. Art Unit TBA Examiner Name TBA Attorney Docket Number 73591	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>					
Sheet	1	of	2		

[illegible]

Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04.

³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

document under WFO or Standard O. If not possible, Applicant is to place a checkmark here if English language translation is required.
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Substitute for form 1449B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>		Complete if Known			
		Application Number	10/065,209		
		Filing Date	9/25/2002		
		First Named Inventor	Longden et al.		
		Group Art Unit	TBA		
		Examiner Name	TBA		
Sheet	2	of	2	Attorney Docket Number	73591

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite, No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	²
		"Electronics Packaging and Production", p 26-27	
		Electronic Materials and Processes, Consulting and Short Courses:, p 1-3	
		"Electronic Materials Handbook", p 470-483	
		C. Harper, "Electronic Packaging and Interconnection Handbook", McGraw Hill p 6.41-6.49	
		M. P. Baze et al., "Latch-up Paths in Bipolar Integrated Circuits", IEEE Transactions on Nuclear Science, December 1986, Vol. NS-33 No. 6	
		A. H. Johnston et al., "The Effect of Temperature on Single-Particle Latch-Up", IEEE Transactions on Nuclear Science, December 1991, Vol. 38 No. 6	
		Song et al., "Parametric Investigation of Latch-Up Sensitivity in 1.25 CMOS Technology", IEEE Transactions on Nuclear Science, December 1987, Vol. NS-34 No. 6	
		D. G. Millward et al., "The Effectiveness of RAD-PAK ICs for Space Radiation Hardening, 1990 Proceedings 40 th Electronic Components and Technology Conference IEEE, Vol. 2 pp 913-916, 1990.	
		C. Harper, "Electronic Packaging and Interconnection Handbook", McGraw Hill 1997, p 6.34	

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